mask. To prevent an influence of plasma damage or an influence occurring when the fourth contact **27** pierces through the third wire **24** during the etching, it is desirable to form the fourth contact **27** on the third wire **24** except for a region right above the second memory cell hole **17**. Although the fourth contact **27** is drawn as being located right above the second memory cell hole **17** in FIG. **10**, it is formed in a region except for the region right above the second memory cell hole **17** in a depth direction.

[0147] Finally, as shown in FIG. **10**(*c*), the upper wires **13** are formed on the fourth interlayer insulating layer **25** using a desired mask such that each upper wire **13** is connected to the third contact **26** and the fourth contact **27**. The upper wires **13** are made of the material similar to the material of the first wires **2**. After that, an insulating protective layer (not shown) is formed, thereby manufacturing the nonvolatile semiconductor memory device according to Embodiment 2 of the present invention as shown in FIG. **2**

[0148] Numeral modifications and alternative embodiments of the present invention will be apparent to those skilled in the art in view of the foregoing description. Accordingly, the description is to be construed as illustrative only, and is provided for the purpose of teaching those skilled in the art the best mode of carrying out the invention. The details of the structure and/or function may be varied substantially without departing from the spirit of the invention.

INDUSTRIAL APPLICABILITY

[0149] The present invention relates to a cross-point nonvolatile semiconductor memory device using diode elements and resistance variable layers, and achieves a nonvolatile memory having a very large memory capacity. Therefore, the present invention is useful in fields of various electronic hardware using nonvolatile memory devices.

1. A nonvolatile semiconductor memory device comprising:
- a substrate;
- first wires of a stripe shape which are formed on the substrate;
- a first interlayer insulating layer formed over the first wires;
- first memory cell holes formed in the first interlayer insulating layer on the first wires;
- first resistance variable layers which are connected to the first wires via the first memory cell holes, respectively;
- first non-ohmic elements formed on the first resistance variable layers, respectively;
- second wires of a stripe shape which are formed on the first interlayer insulating layer such that the second wires respectively cross the first wires so as to be perpendicular to the first wires;
- a second interlayer insulating layer formed over the second wires; and
- upper wires formed on the second interlayer insulating layer;
  - wherein each of the second wires has a plurality of layers including at least a portion of the first non-ohmic element and has an electrically-conductive layer in an uppermost layer of the second wire and a semiconductor layer or an insulator layer which is a portion of the non-ohmic element in a lowermost layer of the second wire;
  - wherein each of the first wires is connected to the upper wire via a first contact penetrating the first interlayer insulating layer and the second interlayer insulating layer;
  - and wherein the uppermost layer of each of the second wires is connected to the upper wire via a second contact penetrating the second interlayer insulating layer.

2. A nonvolatile semiconductor memory device comprising:
- a substrate;
- first wires of a stripe shape which are formed on the substrate;
- a first interlayer insulating layer formed over the first wires;
- first memory cell holes formed in the first interlayer insulating layer on the first wires;
- first resistance variable layers which are connected to the first wires via the first memory cell holes, respectively;
- first non-ohmic elements formed on the first resistance variable layers, respectively;
- second wires of a stripe shape which are formed on the first interlayer insulating layer such that the second wires respectively cross the first wires to be perpendicular to the first wires;
  - a second interlayer insulating layer formed over the second wires;
  - a third interlayer insulating layer formed over the second interlayer insulating layer;
  - second memory cell holes penetrating the second interlayer insulating layer and the third insulating layer on the second wires;
  - second resistance variable layers connected to the second wires via the second memory holes, respectively;
  - second non-ohmic elements formed on the second resistance variable layers, respectively;
  - third wires of a stripe shape which are formed on the third interlayer insulating layer such that the third wires respectively cross the second wires so as to be perpendicular to the second wires;
  - a fourth interlayer insulating layer formed over the third wires; and
  - upper wires formed on the fourth interlayer insulating layer;
  - wherein each of the second wires has a plurality of layers including at least a portion of the first non-ohmic element and has an electrically-conductive layer in an uppermost layer of the second wire and a semiconductor layer or an insulator layer which is a portion of the first non-ohmic element in a lowermost layer of the second wire, and each of the third wires has a plurality of layers including at least a portion of the second non-ohmic element and has an electrically-conductive layer in an uppermost layer of the third wire and a semiconductor layer or an insulator layer which is a portion of the second non-ohmic element in a lowermost layer of the third wire;
  - wherein the uppermost layer of each of the second wires is connected to the upper wire via a stacked contact including a second contact penetrating the second interlayer insulating layer and the third contact penetrating the third interlayer insulating layer and the fourth interlayer insulating layer, the second contact and the third contact being stacked together;